CLAIMS

1. A glitch removal circuit, comprising:

a delay circuit that receives an input signal and generates first and second delayed input signals;

a glitch blocking circuit, coupled to the delay circuit, for removing both positive and negative glitches from the input signal, the glitch blocking circuit comprising:

a first PMOS transistor receiving the input signal;

a first NMOS transistor receiving the input signal;

a second PMOS transistor receiving the first delayed input signal; and

a second NMOS transistor receiving the first delayed input signal; and

a latch circuit, having an input coupled to an output of the glitch blocking circuit, for providing a generally glitch free signal.

2. The glitch removal circuit according to claim 1, wherein the delay circuit comprises at least one transmission gate.

3. The glitch removal circuit according to claim 1, wherein the delay circuit comprises:

first and second inverters connected in series, the first inverter receiving the input signal and the second inverter generating the first delayed input signal and ;

a third inverter having an input connected to the output of the second inverter, the third inverter generating the second delayed input signal.

4. The glitch removal circuit according to claim 3, wherein the glitch blocking circuit comprises:

the first PMOS transistor having a gate receiving the input signal;

the first NMOS transistor having a gate receiving the input signal, a drain connected to a drain of the first PMOS transistor, and wherein the output of the glitch blocking circuit is derived from the drain of the first NMOS transistor;

the second PMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first PMOS transistor, and a source receiving the second delayed input signal; and

the second NMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first NMOS transistor, and a source receiving the second delayed input signal.

5. The glitch removal circuit according to claim 4, wherein the latch circuit comprises:

a fourth inverter having an input connected to the output of the glitch blocking circuit; and

a fifth inverter having an input connected to an output of the fourth inverter, and an output connected to the input of the fourth inverter, wherein the generally glitch free signal is derived from the output of the fourth inverter.

6. The glitch removal circuit according to claim 3, wherein the glitch blocking circuit further comprises:

a third PMOS transistor having a gate connected to the source of the first NMOS transistor, a source connected to ground, and a drain connected to the source of the first PMOS transistor; and

a third NMOS transistor having a gate connected to the source of the first PMOS transistor, a source connected to a

reset voltage, and a drain connected to the source of the first NMOS transistor.

7. The glitch removal circuit according to claim 6, wherein the latch circuit comprises an inverter having an input connected to the output of the glitch blocking circuit.

8. A glitch removal circuit for removing positive and negative glitches from an input signal, comprising:

a delay circuit having first and second inverters connected in series, the first inverter receiving the input signal and the second inverter generating a first delayed input signal, and a third inverter having an input connected to the output of the second inverter, the third inverter generating a second delayed input signal;

a glitch blocking circuit, coupled to the delay circuit, for removing both positive and negative glitches from the input signal, the glitch blocking circuit comprising:

a first PMOS transistor having a gate receiving the input signal;

a first NMOS transistor having a gate receiving the input signal, a drain connected to a drain of the first PMOS transistor, and wherein an output of the glitch blocking circuit is derived from the drain of the first NMOS transistor;

a second PMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first PMOS transistor, and a source receiving the second delayed input signal; and

a second NMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of

the first NMOS transistor, and a source receiving the second delayed input signal; and

a latch circuit including a fourth inverter having an input connected to the output of the glitch blocking circuit and a fifth inverter having an input connected to an output of the fourth inverter and an output connected to the input of the fourth inverter, wherein a generally glitch free signal is derived from the output of the fourth inverter.

9. A glitch removal circuit, comprising:

a delay circuit that receives an input signal and generates first and second delayed input signals;

a glitch blocking circuit, coupled to the delay circuit, for removing both positive and negative glitches from the input signal, the glitch blocking circuit comprising:

first and second NMOS transistors coupled to the delay circuit for receiving the first delayed input signal; and

first and second PMOS transistors coupled to the delay circuit; and

a latch circuit, having an input coupled to an output of the glitch blocking circuit, for providing a generally glitch free signal.

10. The glitch removal circuit according to claim 9, wherein the delay circuit comprises:

a first inverter having an input receiving the input signal and an output providing the first delayed input signal;

second and third inverters connected in series, the second inverter receiving the input signal and the third inverter providing the second delayed output signal.

11. The glitch removal circuit according to claim 10, wherein the glitch blocking circuit comprises:

the first PMOS transistor having a gate receiving the first delayed input signal;

the first NMOS transistor having a gate receiving the first delayed input signal and a drain connected to a drain of the first PMOS transistor;

the second PMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first PMOS transistor, and a drain connected to the delay circuit and receiving the second delayed input signal; and

the second NMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first NMOS transistor, and a drain connected to the delay circuit and receiving the second delayed input signal, wherein an output of the glitch blocking circuit is derived from the drain of the first NMOS transistor.

12. The glitch removal circuit according to claim 11, wherein the latch circuit comprises:

a fourth inverter having an input connected to the output of the glitch blocking circuit; and

a fifth inverter having an input connected to an output of the fourth inverter, and an output connected to the input of the fourth inverter, wherein the generally glitch free signal is derived from the output of the fourth inverter.

13. The glitch removal circuit of claim 11, wherein the glitch blocking circuit further comprises:

a third PMOS transistor having a gate connected to the source of the first NMOS transistor, a source connected to

ground, and a drain connected to the source of the first PMOS transistor; and

a third NMOS transistor having a gate connected to the source of the first PMOS transistor, a source connected to a reset voltage, and a drain connected to the source of the first NMOS transistor.

14. The glitch removal circuit according to claim 13, wherein the latch circuit comprises an inverter having an input connected to the output of the glitch blocking circuit.

15. The glitch removal circuit according to claim 9, wherein the delay circuit comprises:

first and second inverters connected in series, the first inverter receiving the input signal and generating the first delayed output signal and the second inverter providing the second delayed output signal.

16. The glitch removal circuit according to claim 15, wherein the glitch blocking circuit comprises:

the first PMOS transistor having a gate receiving the first delayed input signal;

the first NMOS transistor having a gate receiving the first delayed input signal and a drain connected to a drain of the first PMOS transistor;

the second PMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first PMOS transistor, and a drain connected to the delay circuit and receiving the second delayed input signal; and

the second NMOS transistor having a gate receiving the first delayed input signal, a drain connected to a source of the first NMOS transistor, and a drain connected to the delay circuit and

receiving the second delayed input signal, wherein an output of the glitch blocking circuit is derived from the drain of the first NMOS transistor.

17. The glitch removal circuit according to claim 16, wherein the latch circuit comprises:

a third inverter having an input connected to the output of the glitch blocking circuit; and

a fourth inverter having an input connected to an output of the third inverter, and an output connected to the input of the third inverter, wherein the generally glitch free signal is derived from the output of the third inverter.

18. The glitch removal circuit according to claim 9, wherein the delay circuit comprises:

a first inverter having an input receiving the input signal and an output providing the first delayed input signal;

second and third inverters connected in series, the second inverter receiving the input signal and providing the second delayed input signal and the third inverter providing a third delayed output signal.

19. The glitch removal circuit according to claim 18, wherein the glitch blocking circuit comprises:

the first PMOS transistor having a gate receiving the first delayed input signal;

the first NMOS transistor having a gate receiving the first delayed input signal and a drain connected to a drain of the first PMOS transistor;

the second PMOS transistor having a gate receiving the second delayed input signal, a drain connected to a source of the

first PMOS transistor, and a drain connected to the delay circuit and receiving the third delayed input signal; and

the second NMOS transistor having a gate receiving the second delayed input signal, a drain connected to a source of the first NMOS transistor, and a drain connected to the delay circuit and receiving the third delayed input signal, wherein an output of the glitch blocking circuit is derived from the drain of the first NMOS transistor.

20. The glitch removal circuit according to claim 19, wherein the latch circuit comprises:

a fourth inverter having an input connected to the output of the glitch blocking circuit; and

a fifth inverter having an input connected to an output of the fourth inverter, and an output connected to the input of the fourth inverter, wherein the generally glitch free signal is derived from the output of the fourth inverter.

21. A method for removing both positive and negative glitches from an input signal to generate a glitch free signal, using a glitch blocking circuit, wherein the glitch blocking circuit includes a first PMOS transistor, a second PMOS transistor, a first NMOS transistor and a second NMOS transistor, the glitch removing method comprising:

delaying the input signal to generate a delayed input signal;

applying the input signal to the gates of the first PMOS and first NMOS transistors;

applying the delayed input signal to the gates of the second PMOS and second NMOS transistors;

if the input signal is glitch free, then inverting the output of the glitch blocking circuit and providing the inverted

signal as the glitch free signal and storing the glitch free signal for later use;

if the input signal has a glitch, then switching off the glitch blocking circuit for a duration of the glitch and providing the previously stored glitch free signal as an output.

22. The glitch removal method of claim 21, wherein inverting the output of the glitch blocking circuit comprises:

if the input signal is low, then switching on the first PMOS transistor and the second PMOS transistor and switching off the first NMOS transistor and the second NMOS transistor; and

if the input signal is high, then switching on the first NMOS transistor and the second NMOS transistor and switching off the first PMOS transistor and the second PMOS transistor.

23. The method according to claim 21, wherein switching off the glitch blocking circuit comprises:

if a positive glitch is present, then switching off the first PMOS transistor and the second NMOS transistor and switching on the first NMOS transistor and the second PMOS transistor; and

if a negative glitch is present, then switching off the first NMOS transistor and the second PMOS transistor and switching on the first PMOS transistor and the second NMOS transistor.